LFMC-TTL

Hardware

User Manual

Rev. A1
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Document change history

Version	Description	Date
1.0	First release	24 January 2024

TABLE OF CONTENTS

1 INTRODUCTION

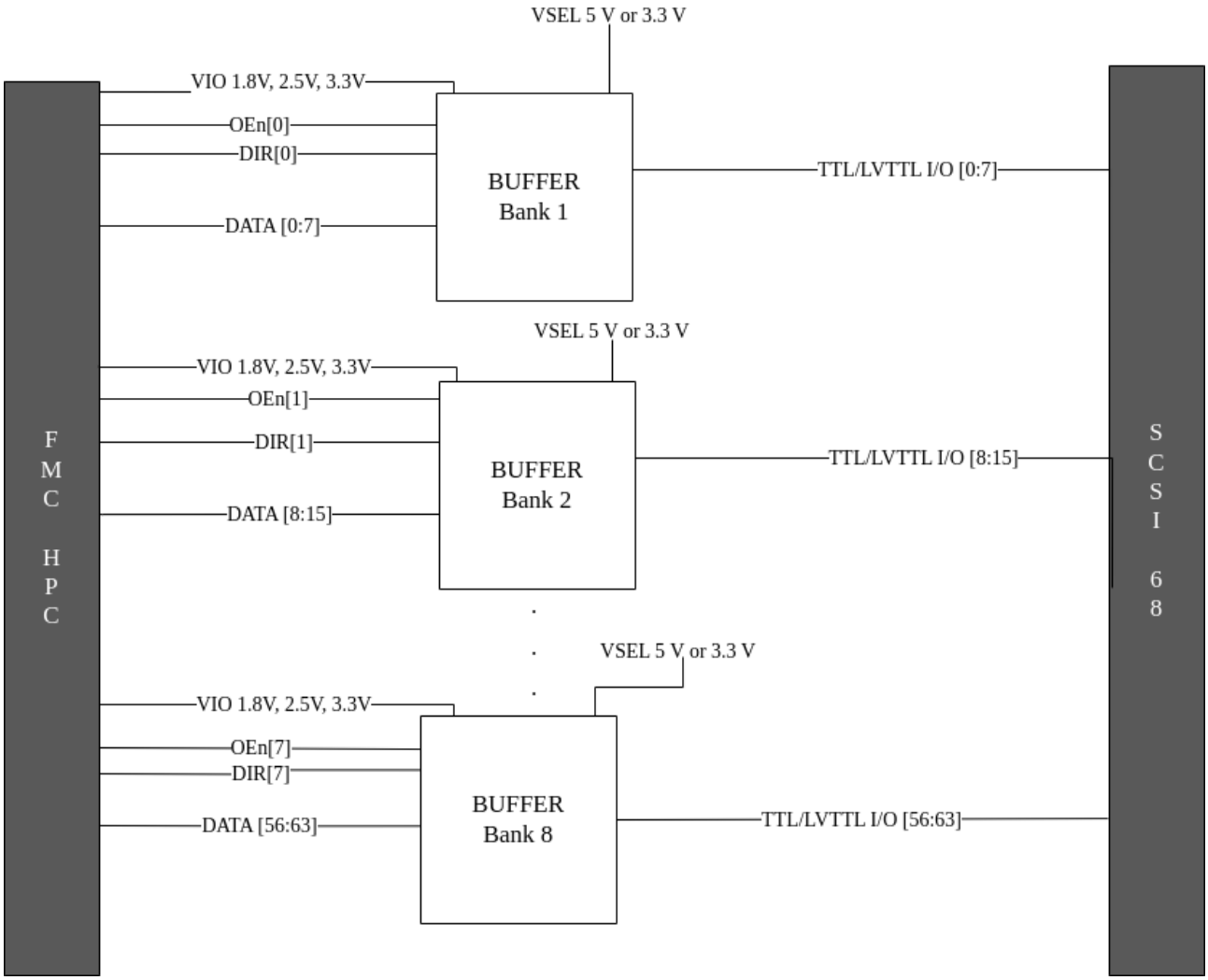
The LFMC-TTL is an FMC (VITA 57) I/O Module which provides 64 TTL/LVTTL bidirectional IO.
The module is made of 8 direction controlled buffers with 8 I/O each. Direction and output enable is configurable per bank.

1.1 SPECIFICATION

There are 8 SN74LXCH8T245PWR buffers installed on the module with the following characteristics:

- Drive strength : 32 mA
- Output voltage : configurable 3.3V or 5V
- Direction control: Controllable via FMC signals, per bank
- Connector: SCSI 68 VHDCI, Part number TE 5796055-1

1.2 BLOCK DIAGRAM



Also the assignment implied by the electrical scheme induces: DIR[0] → Direction signal of buffer U9, DIR[1] → Direction signal of buffer U5, DIR[2] → Direction signal of buffer U8, DIR[3] → Direction signal of buffer U3; DIR[4] → Direction signal of buffer U2, DIR[5] → Direction signal of buffer U4; DIR[6] → Direction signal of buffer U7, DIR[7] → Direction signal of buffer U6

2 INSTALLATION

2.1 FITTING

The LFMC-TTL is designed to plug in the FMC connector of the LVPX-X102 board. The retaining screws should be tightened to secure LFMC-TTL.

> Note: This operation should not be performed while the LVPX-X102 card is powered up.

2.2 CONFIGURATIONS

The use of these boards requires that the FPGA cards are factory-configured to suit.

2.3 HANDLING INSTRUCTIONS

Avoid flexing the board. Avoid to drop impurities on the board as this may interfer with its functionality, e.g. some input output channels not working properly.

2.4 VOLTAGE SETTINGS

Possible voltage options for the LFMC-TTL module are 3.3 V and 5 V.
There are J2 and J3 connectors, which control the voltage of the IO for the first 4 TTL buffers and of the last 4 ttl buffers respectively. Thus 2 jumpers are needed to set a voltage option.
The J2/J3 connectors are made by 3 pins [1 2 3]. A jumper can connect [1 2] or [2 3].
For the J2, assuming VOUT_SEL_1 is 3.3 V (which means that the first 4 benches are powered by 3.3 V) then the needed jumper configuration is [2 3], because in the electrical scheme the pin 2 is related to the signal VOUT_SEL_1 and the pin 3 to VCC_3V3.
For the J1, assuming VOUT_SEL_2 is 5 V (which means that the last 4 benches are powered by 5 V) then the needed jumper configuration is [1 2], because the pin 2 is related to VOUT_SEL_2 , and the pin 1 is related to VCC_5V0.

By default, both jumpers are in configuration [2 3], meaning that all 8 benches are powered by 3.3 V.

Strapping options:

Option	J2	J3	VOUT_SEL_1	VOUT_SEL_2
1	[1 2]	[1 2]	5 V	5 V
2	[1 2]	[2 3]	5 V	3.3 V
3	[2 3]	[1 2]	3.3 V	5 V
4	[2 3]	[2 3]	3.3 V	3.3 V

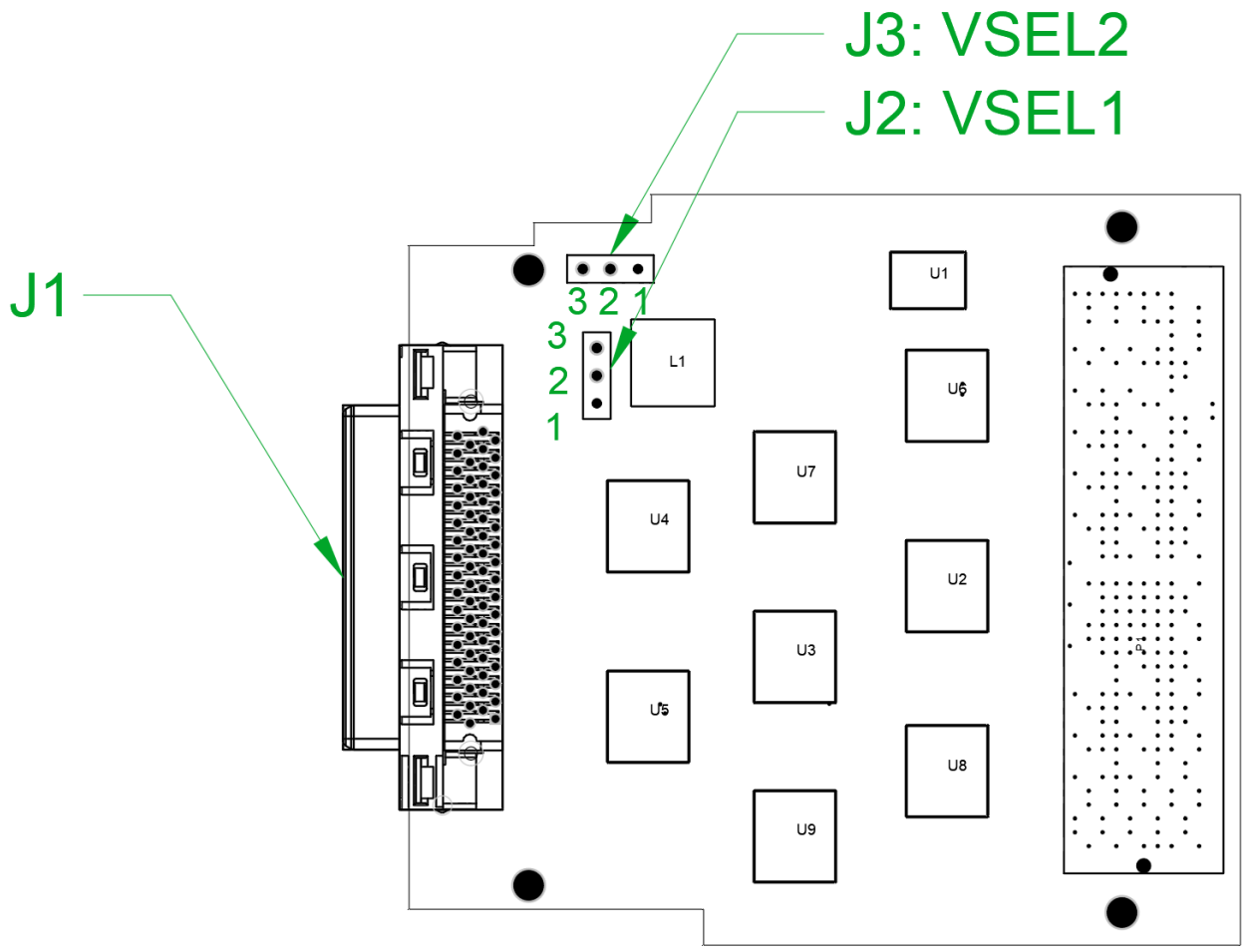


Figure 1: Module Layout

3 INTERFACES

The following signals are used:

Signal	Function	Driver by	Comments
DIR [0..7]	Buffer Direction control (by bank of 8) 0 = B → A 1 = A → B	FPGA	-
OEn [0..7]	Buffer output enable 0 = enabled 1 = disabled	FPGA	-
DATA [0..63]	Input Output Channel 0 = bit 0 transmitted 1 = bit 1 transmitted	Bidirectional, depends on DIR and OEn	-

DIR is a signal which handles direction of data flow, there is one for each TTL buffer. Thus the direction of each buffer is controllable by the FPGA HDL application.

OEn is a signal which establishes whether the output of a TTL buffer is enabled or not (active low) . If the OEn is set to 0 it means that output is enabled. If the direction for that buffer is “0” then the A port of the buffer is output enabled, if the direction is “1” then the B port of the buffer is output enabled.
When OEn is “1” the output is not enabled meaning that the buffer’s configuration is in “Isolation”.

DATA is a signal for data transmission via TTL buffers. Since there are 8 IOs for each buffer, there are a total of 64 input output channels. The data is propagameted from the A port to the B port when DIR signal for that buffer is 1 (Output to SCSI), and from port B to port A when DIR is 0 (Input from SCSI).

Front Panel Connector (SCSI)

PIN	SIGNAL	PIN	SIGNAL
1	GND	**35**	GND
2	DATA 0 (U9 bank #0)	**36**	DATA 1 (U9 bank #0)
3	DATA 2 (U9 bank #0)	**37**	DATA 3 (U9 bank #0)
4	DATA 4 (U9 bank #0)	**38**	DATA 5 (U9 bank #0)
5	DATA 6 (U9 bank #0)	**39**	DATA 7 (U9 bank #0)
6	DATA 8 (U5 bank #1)	**40**	DATA 9 (U5 bank #1)
7	DATA 10 (U5 bank #1)	**41**	DATA 11 (U5 bank #1)
8	DATA 12 (U5 bank #1)	**42**	DATA 13 (U5 bank #1)
9	DATA 14 (U5 bank #1)	**43**	DATA 15 (U5 bank #1)
10	DATA 16 (U8 bank #2)	**44**	DATA 17 (U8 bank #2)
11	DATA 18 (U8 bank #2)	**45**	DATA 19 (U8 bank #2)
12	DATA 20 (U8 bank #2)	**46**	DATA 21 (U8 bank #2)

13	DATA 22 (U8 bank #2)	**47**	DATA 23 (U8 bank #2)
14	DATA 24 (U3 bank #3)	**48**	DATA 25 (U3 bank #3)
15	DATA 26 (U3 bank #3)	**49**	DATA 27 (U3 bank #3)
16	DATA 28 (U3 bank #3)	**50**	DATA 29 (U3 bank #3)
17	DATA 30 (U3 bank #3)	**51**	DATA 31 (U3 bank #3)
18	DATA 32 (U2 bank #4)	**52**	DATA 33 (U2 bank #4)
19	DATA 34 (U2 bank #4)	**53**	DATA 35 (U2 bank #4)
20	DATA 36 (U2 bank #4)	**54**	DATA 37 (U2 bank #4)
21	DATA 38 (U2 bank #4)	**55**	DATA 39 (U2 bank #4)
22	DATA 40 (U4 bank #5)	**56**	DATA 41 (U4 bank #5)
23	DATA 42 (U4 bank #5)	**57**	DATA 43 (U4 bank #5)
24	DATA 44 (U4 bank #5)	**58**	DATA 45 (U4 bank #5)
25	DATA 46 (U4 bank #5)	**59**	DATA 47 (U4 bank #5)
26	DATA 48 (U7 bank #6)	**60**	DATA 49 (U7 bank #6)
27	DATA 50 (U7 bank #6)	**61**	DATA 51 (U7 bank #6)
28	DATA 52 (U7 bank #6)	**62**	DATA 53 (U7 bank #6)
29	DATA 54 (U7 bank #6)	**63**	DATA 55 (U7 bank #6)
30	DATA 56 (U6 bank #7)	**64**	DATA 57 (U6 bank #7)
31	DATA 58 (U6 bank #7)	**65**	DATA 59 (U6 bank #7)
32	DATA 60 (U6 bank #7)	**66**	DATA 61 (U6 bank #7)
33	DATA 62 (U6 bank #7)	**67**	DATA 63 (U6 bank #7)
34	GND	**68**	GND

FMC interconnection

TTL Buffer	FMC (P1)	FMC PIN (P1)	SIGNAL
U9	FMC_LA_P[0]	G6	DATA[0]
U9	FMC_LA_N[0]	G7	DATA[1]
U9	FMC_LA_P[1]	D8	DATA[2]
U9	FMC_LA_N[1]	D9	DATA[3]
U9	FMC_LA_P[2]	H7	DATA[4]
U9	FMC_LA_N[2]	H8	DATA[5]
U9	FMC_LA_P[3]	G9	DATA[6]
U9	FMC_LA_N[3]	G10	DATA[7]
U9	FMC_LA_P[4]	H10	DIR_bank0
U9	FMC_LA_N[4]	H11	Oen_bank0
U5	FMC_LA_P[10]	C14	DIR_bank1
U5	FMC_LA_N[10]	C15	Oen_bank1
U5	FMC_LA_P[11]	H16	DATA[8]
U5	FMC_LA_N[11]	H17	DATA[9]
U5	FMC_LA_P[12]	G15	DATA[10]
U5	FMC_LA_N[12]	G16	DATA[11]
U5	FMC_LA_P[13]	D17	DATA[12]
U5	FMC_LA_N[13]	D18	DATA[13]
U5	FMC_LA_P[14]	C18	DATA[14]
U5	FMC_LA_N[14]	C19	DATA[15]

U8	FMC_LA_P[5]	D11	DIR_0_23
U8	FMC_LA_N[5]	D12	Oen_0_23
U8	FMC_LA_P[6]	C10	DATA[16]
U8	FMC_LA_N[6]	C11	DATA[17]
U8	FMC_LA_P[7]	H13	DATA[18]
U8	FMC_LA_N[7]	H14	DATA[19]
U8	FMC_LA_P[8]	G12	DATA[20]
U8	FMC_LA_N[8]	G13	DATA[21]
U8	FMC_LA_P[9]	D14	DATA[22]
U8	FMC_LA_N[9]	D15	DATA[23]
U3	FMC_HA_P[14]	J15	DIR_0_31
U3	FMC_HA_N[14]	J16	Oen_0_31
U3	FMC_HA_P[15]	F16	DATA[24]
U3	FMC_HA_N[15]	F17	DATA[25]
U3	FMC_HA_P[16]	E15	DATA[26]
U3	FMC_HA_N[16]	E16	DATA[27]
U3	FMC_HA_P[17]	K16	DATA[28]
U3	FMC_HA_N[17]	K17	DATA[29]
U3	FMC_HA_P[18]	J18	DATA[30]
U3	FMC_HA_N[18]	J19	DATA[31]
U2	FMC_HA_P[19]	F19	DIR_0_39
U2	FMC_HA_N[19]	F20	Oen_0_39
U2	FMC_HA_P[20]	E18	DATA[32]
U2	FMC_HA_N[20]	E19	DATA[33]
U2	FMC_HA_P[21]	K19	DATA[34]
U2	FMC_HA_N[21]	K20	DATA[35]
U2	FMC_HA_P[22]	J21	DATA[36]
U2	FMC_HA_N[22]	J22	DATA[37]
U2	FMC_HA_P[23]	K22	DATA[38]
U2	FMC_HA_N[23]	K23	DATA[39]
U4	FMC_LA_P[15]	H19	DIR_0_47
U4	FMC_LA_N[15]	H20	Oen_0_47
U4	FMC_LA_P[16]	G18	DATA[40]
U4	FMC_LA_N[16]	G19	DATA[41]
U4	FMC_LA_P[17]	D20	DATA[42]
U4	FMC_LA_N[17]	D21	DATA[43]
U4	FMC_LA_P[18]	C22	DATA[44]
U4	FMC_LA_N[18]	C23	DATA[45]
U4	FMC_LA_P[19]	H22	DATA[46]
U4	FMC_LA_N[19]	H23	DATA[47]
U7	FMC_LA_P[20]	G21	DIR_0_55
U7	FMC_LA_N[20]	G22	Oen_0_55
U7	FMC_LA_P[21]	H25	DATA[48]
U7	FMC_LA_N[21]	H26	DATA[49]
U7	FMC_LA_P[22]	G24	DATA[50]

U7	FMC_LA_N[22]	G25	DATA[51]
U7	FMC_LA_P[23]	D23	DATA[52]
U7	FMC_LA_N[23]	D24	DATA[53]
U7	FMC_LA_P[24]	H28	DATA[54]
U7	FMC_LA_N[24]	H29	DATA[55]
U6	FMC_LA_P[25]	G27	DIR_bank7
U6	FMC_LA_N[25]	G28	Oen_bank7
U6	FMC_LA_P[26]	D26	DATA[56]
U6	FMC_LA_N[26]	D27	DATA[57]
U6	FMC_LA_P[27]	C26	DATA[58]
U6	FMC_LA_N[27]	C27	DATA[59]
U6	FMC_LA_P[28]	H31	DATA[60]
U6	FMC_LA_N[28]	H32	DATA[61]
U6	FMC_LA_P[29]	G30	DATA[62]
U6	FMC_LA_N[29]	G31	DATA[63]

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