LFMC-422

Hardware

User Manual

Rev. A1
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Document change history

Version	Description	Date
1.0	First release	24 January 2024

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1 INTRODUCTION

The LFMC-422 is an FMC HPC (VITA 57.1) I/O Module which provides 16 RS422 RX/TX buffers. The module is made of 16 direction controller buffers with 4 I/O each. The Module is ideal for parallel bus handling and I/O operations.

1.1 SPECIFICATION

There are 16 THVD1424 buffers installed on the module with the following characteristics:

- Max data rate: 20 Mbps
- Half Duplex or full duplex configurable via FMC signal for each buffer
- RX and TX termination controllable via FMC signal for each buffer
- TX and RX enable controllable via FMC signal for each buffer
- Connector: SCSI 68 VHDCI, Part number TE 5796055-1

1.2 BLOCK DIAGRAM

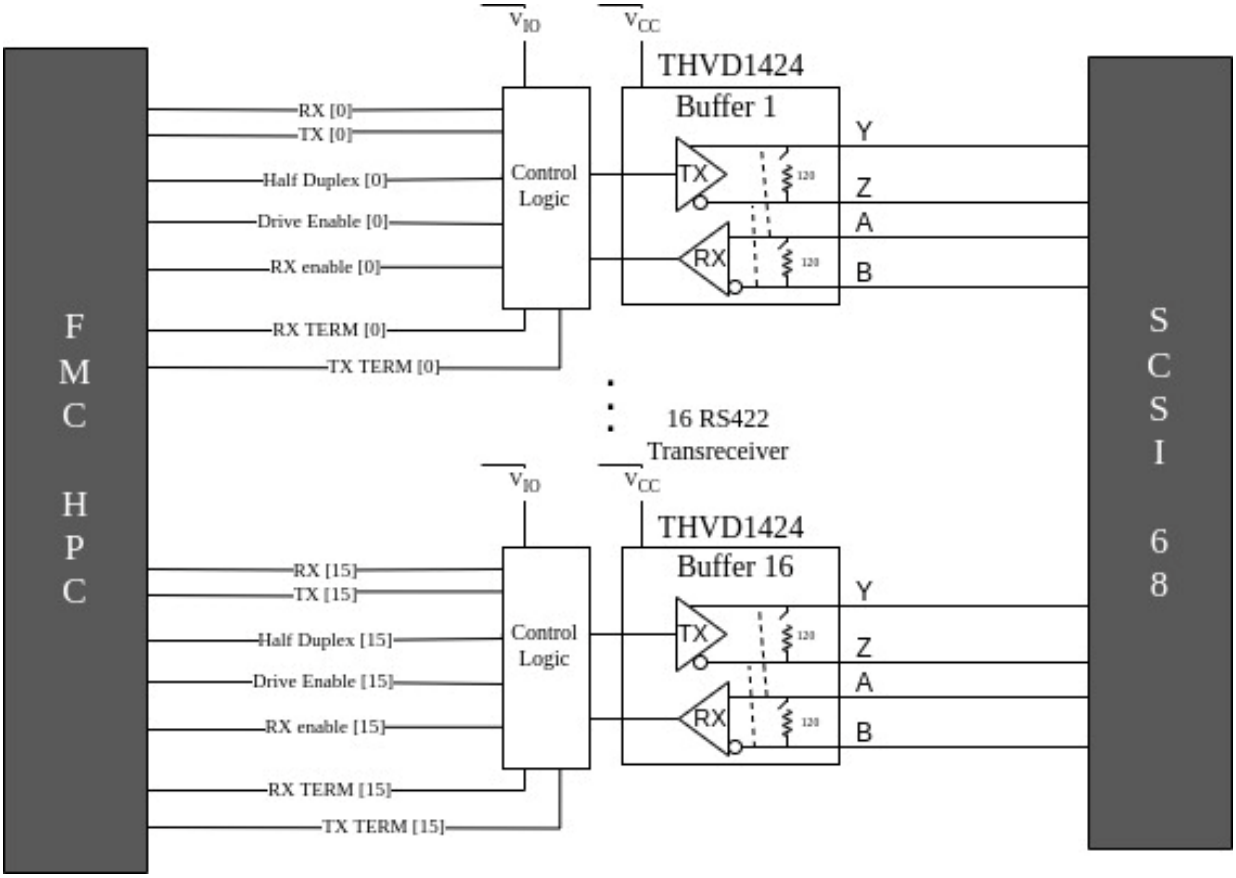

Figure 1: Block diagram

2 INSTALLATION

2.1 FITTING

The LFMC-TTL is designed to plug in the FMC connector of the LVPX-X102 board. The retaining screws should be tightened to secure LFMC-TTL.

> Note: This operation should not be performed while the LVPX-X102 card is powered up.

2.2 CONFIGURATION

The use of these boards requires that the FPGA cards are factory-configured to suit.

2.3 HANDLING INSTRUCTIONS

Avoid flexing the board. Avoid to drop impurities on the board as this may interfer with its functionality, e.g. some input output channels not working properly.

2.4 VOLTAGE SETTINGS

For all the buffers V_{IO} is 1.8 to 3.3 V logic supply voltage.

3 INTERFACES

The following signal are used:

Signal	Function	Driven by	Comments
REn	Receiver enable/disable (default) 0 → enabled 1 → disabled	FPGA	-
DE	Driver enable/disable (default) 0 → disabled 1 → enabled	FPGA	-
H/Fn	Control half and full duplex function. 0 → Full duplex 1 → Half duplex	FPGA	Full duplex default is Y/Z are driver output, A/B are receiver input pins
RX	Receiver channel (output to FPGA)	Buffer	-
TX	Transmitter channel (input from FPGA)	FPGA	-
TERM_TX	Termination of Transmitter.	FPGA	Termination across Y/Z is disabled by default.
TERM_RX	Termination of Receiver.	FPGA	Termination across A/B is disabled by default.

REn is a signal which enables/disables the receiver capability to receive data.
DE controls the transmitter output enable.
In half duplex mode only the couple Y,Z is for both receiving and transmitting. In full duplex also the couple A,B is used. When termination is enabled, the termination resistor of 120 Ohm is connected. Termination can be enabled for TX, RX, none or both, individually for each buffer.

Front Panel Connector (SCSI)

PIN	SIGNAL	PIN	SIGNAL
1	GND	**35**	GND
2	RX0+	**36**	RX0-
3	TX0+	**37**	TX0-
4	RX1+	**38**	RX1-
5	TX1+	**39**	TX1-
6	RX2+	**40**	RX2-
7	TX2+	**41**	TX2-
8	RX3+	**42**	RX3-

9	TX3+	**43**	TX3-
10	RX4+	**44**	RX4-
11	TX4+	**45**	TX4-
12	RX5+	**46**	RX5-
13	TX5+	**47**	TX5-
14	RX6+	**48**	RX6-
15	TX6+	**49**	TX6-
16	RX7+	**50**	RX7-
17	TX7+	**51**	TX7-
18	RX8+	**52**	RX8-
19	TX8+	**53**	TX8-
20	RX9+	**54**	RX9-
21	TX9+	**55**	TX9-
22	RX10+	**56**	RX10-
23	TX10+	**57**	TX10-
24	RX11+	**58**	RX11-
25	TX11+	**59**	TX11-
26	RX12+	**60**	RX12-
27	TX12+	**61**	TX12-
28	RX13+	**62**	RX13-
29	TX13+	**63**	TX13-
30	RX14+	**64**	RX14-
31	TX14+	**65**	TX14-
32	RX15+	**66**	RX15-
33	TX15+	**67**	TX15-
34	GND	**68**	GND

FMC interconnection

422 Buffer	FMC (P1)	FMC PIN (P1)	SIGNALS
U17	FMC_LA_n[0]	G7	tx[0]
U17	FMC_LA_p[0]	G6	rx[0]
U17	FMC_HA_p[0]	F4	de[0]
U17	FMC_HA_n[0]	F5	half_dplx[0]
U17	FMC_HA_p[1]	E2	re_n[0]
U17	FMC_LA_n[1]	D9	tx_term[0]
U17	FMC_LA_p[1]	D8	rx_term[0]
U4	FMC_LA_n[2]	H8	tx[1]
U4	FMC_LA_p[2]	H7	rx[1]
U4	FMC_HA_p[2]	K7	de[1]
U4	FMC_HA_n[2]	K8	half_dplx[1]
U4	FMC_HA_p[3]	J6	re_n[1]
U4	FMC_LA_n[3]	G10	tx_term[1]

U4	FMC_LA_p[3]	G9	rx_term[1]
U10	FMC_LA_n[4]	H11	tx[2]
U10	FMC_LA_p[4]	H10	rx[2]
U10	FMC_HA_p[4]	F7	de[2]
U10	FMC_HA_n[4]	F8	half_dplx[2]
U10	FMC_HA_p[5]	E6	re_n[2]
U10	FMC_LA_n[5]	D12	tx_term[2]
U10	FMC_LA_p[5]	D11	rx_term[2]
U9	FMC_LA_n[6]	C11	tx[3]
U9	FMC_LA_p[6]	C10	rx[3]
U9	FMC_HA_p[6]	K10	de[3]
U9	FMC_HA_n[6]	K11	half_dplx[3]
U9	FMC_HA_p[7]	J9	re_n[3]
U9	FMC_LA_n[7]	H14	tx_term[3]
U9	FMC_LA_p[7]	H13	rx_term[3]
U8	FMC_LA_n[8]	G13	tx[4]
U8	FMC_LA_p[8]	G12	rx[4]
U8	FMC_HA_p[8]	F10	de[4]
U8	FMC_HA_n[8]	F11	half_dplx[4]
U8	FMC_HA_p[9]	E9	re_n[4]
U8	FMC_LA_n[9]	D15	tx_term[4]
U8	FMC_LA_p[9]	D14	rx_term[4]
U7	FMC_LA_n[10]	C15	tx[5]
U7	FMC_LA_p[10]	C14	rx[5]
U7	FMC_HA_p[10]	K13	de[5]
U7	FMC_HA_n[10]	K14	half_dplx[5]
U7	FMC_HA_p[11]	J12	re_n[5]
U7	FMC_LA_n[11]	H17	tx_term[5]
U7	FMC_LA_p[11]	H16	rx_term[5]
U6	FMC_LA_n[12]	G16	tx[6]
U6	FMC_LA_p[12]	G15	rx[6]
U6	FMC_HA_p[12]	F13	de[6]
U6	FMC_HA_n[12]	F14	half_dplx[6]
U6	FMC_HA_p[13]	E12	re_n[6]
U6	FMC_LA_n[13]	D18	tx_term[6]
U6	FMC_LA_p[13]	D17	rx_term[6]
U5	FMC_LA_n[16]	G19	tx[7]
U5	FMC_LA_p[16]	G18	rx[7]
U5	FMC_HA_p[16]	E15	de[7]
U5	FMC_HA_n[16]	E16	half_dplx[7]
U5	FMC_HA_p[17]	K16	re_n[7]
U5	FMC_LA_n[17]	D21	tx_term[7]
U5	FMC_LA_p[17]	D20	rx_term[7]

U16	FMC_LA_n[14]	C19	tx[8]
U16	FMC_LA_p[14]	C18	rx[8]
U16	FMC_HA_p[14]	J15	de[8]
U16	FMC_HA_n[14]	J16	half_dplx[8]
U16	FMC_HA_p[15]	F16	re_n[8]
U16	FMC_LA_n[15]	H20	tx_term[8]
U16	FMC_LA_p[15]	H19	rx_term[8]
U15	FMC_LA_n[18]	C23	tx[9]
U15	FMC_LA_p[18]	C22	rx[9]
U15	FMC_HA_p[18]	J18	de[9]
U15	FMC_HA_n[18]	J19	half_dplx[9]
U15	FMC_HA_p[19]	F19	re_n[9]
U15	FMC_LA_n[19]	H23	tx_term[9]
U15	FMC_LA_p[19]	H22	rx_term[9]
U14	FMC_LA_n[20]	G22	tx[10]
U14	FMC_LA_p[20]	G21	rx[10]
U14	FMC_HA_p[20]	E18	de[10]
U14	FMC_HA_n[20]	E19	half_dplx[10]
U14	FMC_HA_p[21]	K19	re_n[10]
U14	FMC_LA_n[21]	H26	tx_term[10]
U14	FMC_LA_p[21]	H25	rx_term[10]
U13	FMC_LA_n[22]	G25	tx[11]
U13	FMC_LA_p[22]	G24	rx[11]
U13	FMC_HA_p[22]	J21	de[11]
U13	FMC_HA_n[22]	J22	half_dplx[11]
U13	FMC_HA_p[23]	K22	re_n[11]
U13	FMC_LA_n[23]	D24	tx_term[11]
U13	FMC_LA_p[23]	D23	rx_term[11]
U12	FMC_LA_n[24]	H29	tx[12]
U12	FMC_LA_p[24]	H28	rx[12]
U12	FMC_HB_p[15]	J33	de[12]
U12	FMC_HB_n[15]	J34	half_dplx[12]
U12	FMC_HB_p[14]	K34	re_n[12]
U12	FMC_LA_n[25]	G28	tx_term[12]
U12	FMC_LA_p[25]	G27	rx_term[12]
U11	FMC_LA_n[26]	D27	tx[13]
U11	FMC_LA_p[26]	D26	rx[13]
U11	FMC_HB_p[17]	K37	de[13]
U11	FMC_HB_n[17]	K38	half_dplx[13]
U11	FMC_HB_p[16]	F34	re_n[13]
U11	FMC_LA_n[27]	C27	tx_term[13]
U11	FMC_LA_p[27]	C26	rx_term[13]
U2	FMC_LA_n[28]	H32	tx[14]
U2	FMC_LA_p[28]	H31	rx[14]

U2	FMC_HB_p[19]	E33	de[14]
U2	FMC_HB_n[19]	E34	half_dplx[14]
U2	FMC_HB_p[18]	J36	re_n[14]
U2	FMC_LA_n[29]	G31	tx_term[14]
U2	FMC_LA_p[29]	G30	rx_term[14]
U3	FMC_LA_n[30]	H35	tx[15]
U3	FMC_LA_p[30]	H34	rx[15]
U3	FMC_HB_p[20]	F37	de[15]
U3	FMC_HB_n[20]	F38	half_dplx[15]
U3	FMC_HB_p[21]	E36	re_n[15]
U3	FMC_LA_n[31]	G34	tx_term[15]
U3	FMC_LA_p[31]	G33	rx_term[15]

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